L Number	Hits	Search Text	DB	Time stamp
Number_1	7880	associative near6 (cache memory storage)	USPAT;	2003/08/20
•	7000	associative near (caone memory storage)	US-PGPUB;	17:04
			EPO; JPO;	
			DERWENT	
2	119	(controller logic circuit) same multiplexer	USPAT;	2003/08/20
-		same (associative near6 (cache memory	US-PGPUB;	17:21
		storage))	EPO; JPO;	17.21
		storage))	DERWENT	
3	43	(read\$3 load\$3) near4 (buffer register) and	USPAT;	2003/08/20
J	43	, , , , , , , , , , , , , , , , , , , ,	US-PGPUB;	17:21
		((controller logic circuit) same multiplexer	•	17:21
		same (associative near6 (cache memory	EPO; JPO;	
_		storage)))	DERWENT	0000/00/00
5	14	(concurrently simultaneous parallel	USPAT;	2003/08/20
		("SAME" adj3 time)) same ((controller logic	US-PGPUB;	17:20
		circuit) same multiplexer same (associative	EPO; JPO;	
		near6 (cache memory storage)))	DERWENT	•
6	84	(concurrently simultaneous parallel	USPAT;	2003/08/20
		("SAME" adj3 time)) and ((controller logic	US-PGPUB;	17:21
		circuit) same multiplexer same (associative	EPO; JPO;	
		near6 (cache memory storage)))	DERWENT	
7	513756	(controller logic circuit) same (concurrently	USPAT;	2003/08/20
		simultaneous parallel ("SAME" adj3 time))	US-PGPUB;	17:21
			EPO; JPO;	
			DERWENT	
8	38490	(controller logic circuit) same (concurrently	USPAT;	2003/08/20
		simultaneous parallel ("SAME" adj3 time))	US-PGPUB;	17:22
		same enabl\$3	EPO; JPO;	
			DERWENT	
9	272	(read\$3 load\$3) near4 (buffer register) and	USPAT;	2003/08/20
		(associative near6 (cache memory storage))	US-PGPUB;	17:23
		and ((controller logic circuit) same	EPO; JPO;	
		(concurrently simultaneous parallel	DERWENT	
		("SAME" adj3 time)) same enabl\$3) and	DERWENT	
		multiplexer		
10	172	(read\$3 load\$3) near4 (buffer register) and	USPAT;	2003/08/20
	'/2	(associative near6 (cache memory storage))	US-PGPUB;	17:24
		, , , , , , , , , , , , , , , , , , , ,	EPO; JPO;	17.24
		and ((controller logic circuit) same	1 · ·	
		(concurrently simultaneous parallel	DERWENT	
		("SAME" adj3 time)) same enabl\$3) and		
4.4		(multiplexer with (input\$4 output\$4))		0000/05/55
11	60	711/\$.ccls. and ((read\$3 load\$3) near4	USPAT;	2003/08/20
		(buffer register) and (associative near6	US-PGPUB;	17:24
		(cache memory storage)) and ((controller	EPO; JPO;	
		logic circuit) same (concurrently	DERWENT	
		simultaneous parallel ("SAME" adj3 time))		
	1	same enabl\$3) and (multiplexer with		
		(input\$4 output\$4)))		